REMARKS

By this amendment, claims 1,2, 4, 7-9, 11 and 14-18 have been amended to more clearly define the present application. Care has been exercised to avoid introduction of new matter.

Claim Rejections:

Claim 11 is rejected under 35 U.S.C. §112, first paragraph, as non-enabling.

Claim 11 has been amended for clarity. It is respectfully submitted that the specification on pages 13 and 14 in view of, e.g., Fig 8(a), clearly allows one of skilled in the art to practice the formation of channel regions with different channel lengths (i.e., one is longer than the other).

Claims 7 and 14 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

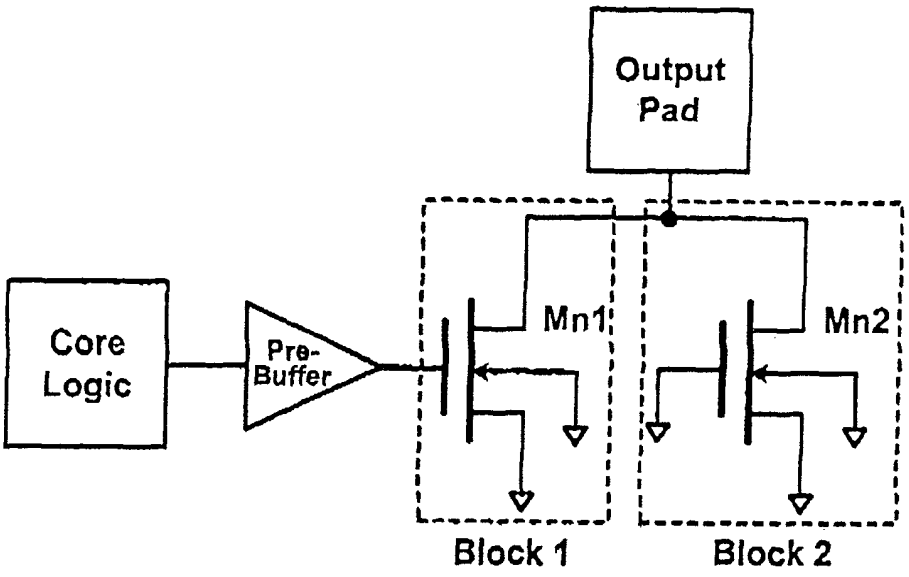
Claims 7 and 14 have been amended to address the concerns as set forth in item 5, page 2 of the outstanding Action.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by *Ker et al.* (USPN 5,637,900, hereinafter "*Ker*").

Before turning to ***Ker*** specifically, a brief discussion and illustration of the difference between the conventional art such as ***Ker***, which teaches enhancing the turn-on speed of the ESD protection devices/circuits, and the present invention as set forth in the claims, which requires restraining of the turn-on speed of the ESD guarded devices/circuits, is in order.

In Exhibit A as shown below, Block 1 is an ESD guarded (protected) block, and block 2 is an ESD protection block. Conventional art teaches making block 2 to turn-on faster to bypass the ESD current, so that block 1 can be protected safely.

Exhibit A



By contrast, instead of focusing on block 2, the present invention as set forth in the claims require restraining the turn-on of block 1 so that block 2 is turned-on before block 1.

Referring specifically to ***Ker***, the N+ and P+ guard rings 710 and 720 are used to prevent VDD-to-VSS latchup. For instance, the MOS transistors as shown in Fig. 8 are used as ESD protection devices to enhance the turn-on behavior. The function of the ESD protection devices would fail unless they can be turned-on in time to prevent others from ESD damage. In other words, the pick-up regions in ***Ker*** are not used in order to realize a turn-on restrain structure.

By contrast, the present invention as now set forth in claim 1 and 2 requires a semiconductor structure that restrains the turn-on behavior.

Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

Claim 5 also recites a semiconductor structure that requires the turn-on behavior of the device restrained. Therefore, claim 5 is distinguishable over ***Ker*** for at least the reasons stated above with respect to claim 1.

Additionally, the P2 MOS transistor of ***Ker*** is a thick-oxide device with a channel length intrinsically longer than the channel length of a general thin-oxide MOS transistor P5 (see Fig. 8 of ***Ker***). The circuit operation principle of ***Ker*** as shown in Fig. 8 requires that the turn-on of P2 MOS transistor be enhanced through P5 MOS transistor, rather than restrained as required by the claimed invention.

Claims 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

Claim 8 from which claim 9 depends also recites a semiconductor structure that requires the turn-on behavior of the device be restrained. Therefore, claims 8 and 9 are distinguishable over ***Ker*** for at least the reasons stated above with respect to claim 1.

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

Claim 12 is distinguishable over ***Ker*** for at least the reasons stated above with respect to claim 5.

Claims 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

Claims 15-18 are distinguishable over ***Ker*** for at least the reasons stated above with respect to claim 1.

Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by *Ker*.

Claim 9 is distinguishable over ***Ker*** for at least the reasons stated above with respect to claim 1.

Claims 3, 6, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ker* (USPN 5,880,932) in view of Admitted Prior Art (hereinafter "APA").

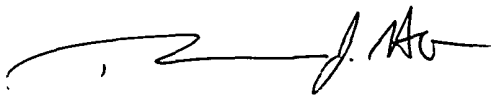
The **APA** does not compensate for the above-discussed deficiency in ***Ker***. Therefore, claims 3, 6, 10 and 13, which further recite features in the semiconductor structure as set forth in claims 1, 5, 8 and 12, are distinguishable over ***Ker*** and **APA**, individually or in combination, for at least the reasons stated above with respect to claims 1, 5, 8 and 12.

In view of the aforementioned amendments and accompanying remarks, claims 1-19 are now in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No.

Respectfully submitted,



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APPENDIX

PROPOSED AMENDMENTS
(version with markings to show changes made)

1. (Amended) A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first region of a second conductivity type within said substrate for forming a drain of a first MOS transistor;

a second region of the second conductivity type within said substrate for forming a source of the first MOS transistor;

a third region of the second conductivity type within said substrate [coupled to a gate] for forming a source of a second MOS transistor, wherein

a fourth region of the first conductivity type is disposed [adjacent to the third region of the second conductivity type] between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to [reduce a] restrain the turn-on [speed or a longer channel length to increase a drain-base breakdown voltage] of said first MOS transistor.

2. (Amended) The semiconductor structure of claim 1, wherein [said fourth region of the first conductivity type is disposed adjacent to the third region of the second conductivity type for surrounding] the channel length of said first MOS transistor is longer than the channel length of said

second MOS transistor to increase the drain-base voltage of said first MOS transistor [with an additional pick-up diffusion to reduce a turn-on speed and a longer channel length to increase a drain-base-breakdown voltage of said first MOS transistor].

4. (Amended) The semiconductor structure of claim 1, further comprising:

a first channel region [of the second conductivity type having a first channel length and] disposed between said first and second regions of said first MOS transistor;

a second channel region [of the second conductivity type having a second channel length and] disposed [between said first and third regions] adjacent to said third region of said second MOS transistor,

wherein said first channel length of said first channel region is longer than the channel length of said second channel region to [is greater than said second channel length to further] increase the drain-base [device] breakdown voltage [for reducing the turn-on speed] of said first MOS transistor.

7. (Amended) The semiconductor structure of claim 5, further comprising a third region of the first conductivity type [adjacent to one] between the source side of said first regions and the source side of said second regions [of said second conductivity type] for surrounding said first MOS transistor with an additional pick-up diffusion to further restrain the turn-on speed of said first MOS transistor.

8. (Amended) A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising:

a p-type substrate of forming a base for said semiconductor structure;

a first N+ region within said substrate for forming a drain of a first MOS transistor;

a second N+ region within said substrate for forming a source of the first MOS transistor;

a third N+ region within said substrate for forming a source [coupled to a gate] of a second MOS transistor, wherein

a P+ region is disposed between the second N+ region of said first MOS transistor and [adjacent to] the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to [reduce a] restrain the turn-on [speed or a longer channel length to increase a drain-base breakdown voltage] of said first MOS transistor.

9. (Amended) The semiconductor structure of claim 8, wherein [said P+ region is disposed adjacent to the third N+ region for surrounding] the channel length of said first MOS transistor [with an additional pick-up diffusion to reduce a turn-on speed and a] is longer than the channel length of said second MOS transistor to increase a drain-base breakdown voltage of said first MOS transistor.

11. (Amended) The semiconductor structure of claim 8, further comprising:

a first n-channel region having a first channel length and disposed between said first and second regions of said first MOS transistor;

a second n-channel region having a second channel length disposed [between said first and second regions] adjacent said third region of said second MOS transistor,

wherein said first channel length is [greater] longer than said second channel length to further [reduce a turn-on speed or a higher] increase the drain-base breakdown voltage of said first MOS transistor.

14. (Amended) The semiconductor structure of claim 12, further comprising a third P+ region between the source region of said first N+ regions and the source region [the first conductivity type adjacent to one] of said second N+ regions for surrounding said first MOS transistor with an additional pick-up diffusion to further restrain the turn-on [speed] of said first MOS transistor.

15. (Amended) A semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input pad and an internal circuit of said integrated circuit comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first channel [of a second conductivity type] formed between [first regions of said second conductivity type] a pair of first regions of a second conductivity type within said substrate for a first MOS transistor; and

a second channel [of the second conductivity type] formed between [second regions of said second conductivity type] formed between a pair of second regions of a second conductivity type within said substrate for a second MOS transistor, wherein

an additional pick-up diffusion region is disposed [adjacent to said first regions of said second conductivity type to reduce a turn-on speed or increase a drain breakdown voltage] between the source region of said first regions and the source region of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

16. (Amended) The semiconductor structure of claim 15, wherein the channel length of said first channel is [greater] longer than the channel length of said second channel to increase a drain-base breakdown voltage of said first MOS transistor.

17. A semiconductor structure for electrostatic discharge (ESD) protection of a high-voltage tolerant I/O cells with stacked NMOS or PMOS integrated circuit, said semiconductor structure connected between a pre-driver circuit and an input/output pad of said integrated circuit and comprising:

a substrate of a first conductivity type forming a base for said semiconductor structure;

a first channel [of a second conductivity type formed between first regions of said second conductivity type] formed between a pair of first regions of a second conductivity type within said substrate for a first MOS transistor which is stacked on a third MOSFET of a second conductivity type; and

a second channel [of the second conductivity type formed between second regions of said second conductivity type] formed between a pair of second regions of a second conductivity type

within said substrate for a second MOS transistor which is stacked on a fourth MOSFET of a second conductivity type, wherein

an additional pick-up diffusion region is disposed [adjacent to said first regions of said second conductivity type to reduce a turn-on speed and/or a longer channel length to increase a drain-base breakdown voltage] between the source region of said first regions and the source of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

18. (Amended) The semiconductor structure of claim 17, wherein the channel length of said first channel is [greater] longer than the channel length of said second channel to increase the drain-base breakdown voltage of said first MOS transistor.